SPECIFICATION

[Title of the Invention]

METHOD OF MANUFACTURING SEMICONDUCTOR DEVICE INCLUDING STEP OF SELECTIVELY FORMING METAL OXIDE LAYER

[Brief Description of the Drawings]

FIGS. 1 through 3 are sectional views illustrating the processes of a method of manufacturing a semiconductor device according to a first embodiment of the present invention.

FIG. 4 is a sectional view illustrating a process of a method of manufacturing a semiconductor device according to a second embodiment of the present invention.

FIG. 5 is a graph illustrating the result of analyzing a sample manufactured in a test example 1 using an X-ray photoelectron spectroscopy (XPS).

FIG. 6 is a graph illustrating the results of measuring the remnant polarization values with respect to a sample 1 and a sample 2 obtained from a test example 2.

[Detailed Description of the Invention]

[Object of the Invention]

[Technical Field of the Invention and Related Art prior to the Invention]

The present invention relates to a method of manufacturing a semiconductor device, and more particularly, to a method of manufacturing a semiconductor device including the step of selectively forming a metal oxide layer on an insulation layer containing oxygen.

Recently, an approach of forming a capacitor dielectric layer using ferroelectric in a semiconductor memory device has attracted attention. For a non-volatile semiconductor memory device, the remnant polarization (P_r) phenomenon of ferroelectric conforms to the concept of binary memory which is the base of a digital memory device widely used at present. Widely used ferroelectric substance is PZT($Pb(Zr, Ti)O_3$) and SBT($SrBi_2Ta_2O_9$).

One of the most serious problems in forming a capacitor dielectric layer using ferroelectric in a semiconductor memory device is that the ferroelectric characteristic of the ferroelectric used for the capacitor dielectric layer is degraded during an integration process of a semiconductor memory device to be performed after the formation of a capacitor. The problem of a capacitor dielectric layer formed of

ferroelectric which is degraded during an integration process of a semiconductor memory device will be described in detail.

In manufacturing a semiconductor memory device, after a capacitor is formed, an InterLayer Dielectric (ILD) process, an InterMetal Dielectric (IMD) process and a passivation process are performed. During these processes, impurities, in particular, hydrogen, which can degrade a capacitor dielectric layer, can be generated. The generated hydrogen may immediately infiltrate into the capacitor dielectric layer during the processes or gradually infiltrate into the capacitor dielectric layer after it has been introduced into an ILD layer, an IMD layer or a passivation layer, which is formed in corresponding one of the processes described above. As a result, P_r, one of the ferroelectric characteristics of the ferroelectric used for the capacitor dielectric layer, decreases.

For example, when an ILD process is performed to form an interlayer insulation layer of a silicon oxide layer after a ferroelectric capacitor is formed on a semiconductor substrate, the dielectric layer of the capacitor is degraded. In other words, in the ILD process of forming an interlayer insulation layer of a silicon oxide layer using a plasma enhanced chemical vapor deposition (PECVD) method, silane (SiH_4) gas and oxygen (O_2) gas is used as reaction gas, and hydrogen is generated as the by-product of the reaction between the silane gas and the oxygen gas. The generated hydrogen may immediately diffuse into the dielectric layer of the ferroelectric capacitor and degrade the dielectric layer, or may be introduced into an interlayer insulation layer formed from the ILD process and gradually degrade the capacitor dielectric layer. As a result, the P_r value of the capacitor dielectric layer decreases, so the capacitor dielectric layer may lose the ferroelectric characteristics. In the integration of a semiconductor memory device, the problem of degradation of a capacitor dielectric layer does not occur only in an ILD process for forming an interlayer insulation layer but may occur in an IMD process for forming an intermetal insulation layer or in a passivation process for forming a passivation layer.

To over this problem, a conventional method of manufacturing a semiconductor memory device encapsulates a capacitor with an insulation layer. For example, U.S. Patent No. 5,822,175 discloses a method of encapsulating a capacitor with a silicon oxide layer, a doped silicon oxide layer or silicon nitride layer to solve the problem of degradation of a capacitor dielectric layer due to diffusion of hydrogen.

[Technical Goal of the Invention]

The present invention provides a method of manufacturing a semiconductor device including a step of selectively forming a metal oxide layer on an insulation layer containing oxygen among material layers exposed on the entire surface of a semiconductor substrate.

[Structure and Operation of the Invention]

Accordingly to an aspect of the present invention, there is provided a method of manufacturing a semiconductor device. In the method, an insulation layer containing oxygen atoms and having a predetermined portion exposed is provided on a semiconductor substrate. Next, a metal oxide layer having a predetermined thickness is selectively formed on the exposed surface of the insulation layer by subjecting the semiconductor substrate to a metal precursor having reactivity with oxygen.

The insulation layer may be a TiO_2 layer, a SiO_2 layer, a Ta_2O_5 layer, an Al_2O_3 layer, a $BaTiO_3$ layer, a $SrTiO_3$ layer, a (Ba, Sr)TiO_3 layer, a $Bi_4Ti_3O_{12}$ layer, a $PbTiO_3$ layer, a PZT((Pb, La)(Zr, Ti)O_3) layer, a ($SrBi_2Ta_2O_9$)(SBT) layer or a compound layer of some of them.

The metal precursor may contain Al, Ta, Ti, Zr, Mg, Ce, Y, Nb, Hf, Sr or Ca.

The step of selectively forming the metal oxide layer may include the sub-steps of pulsing the metal precursor over the entire surface of the semiconductor substrate, and purging the entire surface of the semiconductor substrate, which has been subjected to the pulsed metal precursor, using inert gas.

The method may further includes the step of thermally treating the metal oxide layer in an oxygen atmosphere after the step of selectively forming the metal oxide layer to stabilize the metal oxide layer so that the dielectric characteristic of the metal oxide layer can be enhanced.

According to another aspect, there is provided a method of manufacturing a semiconductor device. In the method, a capacitor including a lower electrode, a capacitor dielectric layer containing oxygen and an upper electrode is formed on a semiconductor substrate. Next, a metal oxide layer having a predetermined thickness is selectively formed on the exposed surface of the capacitor dielectric layer by subjecting the semiconductor substrate to a metal precursor having reactivity with oxygen.

The step of selectively forming the metal oxide layer may include the sub-steps of pulsing the metal precursor over the entire surface of the semiconductor substrate, and purging the entire surface of the semiconductor substrate, which has been subjected to the pulsed metal precursor, using inert gas.

The step of selectively forming the metal oxide layer may be a step of repeating a cycle until the metal oxide layer is formed to a desired thickness, the cycle being a series of steps comprising the metal precursor pulsing step and the inert gas purging step.

The method may further includes the steps of thermally treating the metal oxide layer, and forming an encapsulating layer of an oxide layer containing metal, the encapsulating layer wrapping the entire surface of the capacitor, after the step of selectively forming the metal oxide layer.

The step of forming the encapsulating layer may includes the steps of pulsing a metal precursor over the entire surface of the semiconductor substrate; purging the entire surface of the semiconductor substrate, which has been subjected to the pulsed metal source gas, using inert gas; pulsing oxygen source gas over the entire surface of the semiconductor substrate which has been purged with the inert gas; and purging the entire surface of the semiconductor substrate, which has been subjected to the pulsed oxygen source gas, using inert gas.

According to still another aspect, there is provided a method of manufacturing a semiconductor device. In the method, an interlayer insulation layer wrapping a predetermined conductive region on a semiconductor substrate and containing oxygen atoms is formed. Next, an opening exposing the conductive region is formed by patterning the interlayer insulation layer. Thereafter, a metal oxide layer having a predetermined thickness is selectively formed on the exposed surface of the interlayer insulation layer by subjecting the semiconductor substrate to a metal precursor having reactivity with oxygen.

The conductive region may be the upper or lower electrode of a capacitor, a gate electrode, a bit line, a word line, or the lower conductive line of a multi-layered interconnection layer.

Hereinafter, embodiments of the present invention will be described in detail with reference to the attached drawings. However, the embodiments of the present inv ntion can be modified into various other forms, and the scope of the present invention must not be interpreted as being restricted to the embodiments. Th

embodiments of the present invention are provided in ord r to more completely explain the present invention to anyon skilled in the art. In the drawings, the same reference numerals denote the same members. Also, when a film is described as being on another film or a semiconductor substrate, it can be directly on the other layer or the semiconductor substrate or an interlayer film can exist therebetween.

<First Embodiment>

In a first embodiment, a method of manufacturing a semiconductor device according to the present invention is applied to a process of encapsulating a capacitor of a semiconductor memory device.

Referring to FIG. 1, to apply a method of manufacturing a semiconductor device according to the present invention to a process of encapsulating a capacitor C of a semiconductor memory device, a semiconductor substrate S, on which the capacitor C having a lower electrode 100, a capacitor dielectric layer 110 and an upper electrode 120 sequentially stacked is formed, is prepared. In addition to the capacitor C, the semiconductor substrate S also includes a device isolation layer 130 for defining an active region; a field effect transistor T including a gate electrode 160 having an underlying gate oxide layer 140 interposed between the gate electrode 160 and the semiconductor substrate S and having nitride spacers 150 on its sidewalls, and source and drain regions 170 and 180; an interlayer insulation layer 180 spread on the device isolation layer 130 and the field effect transistor T; and a contact plug 190 formed within the interlayer insulation layer 180 and electrically connected to the source region 170.

The semiconductor substrate S can be prepared by a typical method. Although not shown, other elements besides the above elements may be further provided on the semiconductor substrate S if necessary. For example, an interface layer can be interposed between the interlayer insulation layer 180 and the lower electrode 100 and between the contact plug 190 and the lower electrode 100. The interface layer may include an adhesive layer and a diffusion preventing layer, which are sequentially stacked. The adhesive layer is a material layer for enhancing the adhesive strength between the interlayer insulation layer 180 and the diffusion preventing layer and between the contact plug 190 and the diffusion preventing layer. For example, the adhesive layer may be a transition metal layer (e.g., a Ti layer). The diffusion prev nting layer prevents a material layer formed on the interface layer from reacting with the contact plug 190 formed under the interface layer during

succeeding processes and prevents the contact plug 190 from being degraded due to the diffusion of oxygen during succeeding processes performed in an oxygen atmosphere. For example, the diffusion preventing layer may be a nitride layer (e.g., a TiN layer) of a transition metal. In addition, a capping insulation layer of a nitride layer may be formed on the surface of the gate electrode 160.

Each of the lower electrode 100 and the upper electrode 120 may be a metal layer, a conductive metal oxide layer or a compound layer of them. Here, the metal layer may be a Pt layer, an Ir layer, a Ru layer, a Rh layer, an Os layer or a Pd layer. The conductive metal oxide layer may be an IrO_2 layer, a RuO_2 layer, a (Ca, Sr)RuO_3 layer or a $LaSrCoO_3$ layer. For example, the lower electrode 100 may be a Pt layer, and the upper electrode 120 may be a double layer in which an IrO_2 layer and an Ir layer are sequentially stacked.

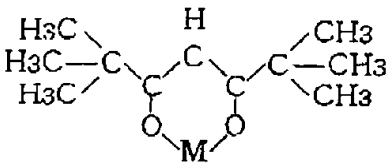
The capacitor dielectric layer 110 may be a TiO_2 layer, a SiO_2 layer, a Ta_2O_5 layer, an Al_2O_3 layer, a $BaTiO_3$ layer, a $SrTiO_3$ layer, a (Ba, Sr)TiO_3 layer, a $Bi_4Ti_3O_{12}$ layer, a $PbTiO_3$ layer, a PZT((Pb, La)(Zr, Ti)O_3) layer, a ($SrBi_2Ta_2O_9$)(SBT) layer or a compound layer of some of them.

Referring to FIG. 2 which is an enlarged view of the part II of FIG. 1, the semiconductor substrate S is loaded in atomic layer deposition equipment (not shown) and is heated to a temperature of 100-400°C, preferably, about 300°C, under a state in which the pressure of a reaction chamber is maintained at 0.1-1 torr. Thereafter, a method of manufacturing a semiconductor device according to the present invention is applied to selectively form a metal oxide layer, for example, an Al_2O_3 layer, on the capacitor dielectric layer 110.

More specifically, an atomic layer deposition process is performed using an aluminum precursor having reactivity with oxygen and inert gas as pulsing gas and purge gas, respectively. First, a metal precursor, e.g., an aluminum precursor, is pulsed over the entire surface of the semiconductor substrate S. For example, the aluminum precursor may be TriMethyl Aluminum (TMA), DiMethylAluminum Hydride (DMAH), DiMethylEthylAmine Alane (DMEAA), TriIsoButylAluminum (TIBA), TriEthyl Aluminum (TEA) or mixed gas of some of them. The pulsing time may be 0.1-2 seconds, and the pulsing flow rate may be 50-300 sccm. The aluminum precursor is preferably pulsed together with carrier gas such as argon gas.

Gas other than the aluminum precursor may be used as the metal precursor for the atomic layer deposition process. For example, $TaCl_5$ or $Ta(OC_2H_5)_4$ may be

used as a tantalum precursor. $TiCl_4$ or $Ti(OC_2H_5)_4$ may be used as a titanium precursor. $ZrCl_4$ may be used as a zirconium precursor. $HfCl_4$ may be used as a hafnium precursor. $Nb(OC_2H_5)_5$ may be used as a niobium precursor. $Mg(thd)_2$ may be used as a magnesium precursor. $Ce(thd)_3$ may be used as a cerium precursor. $Y(thd)_3$ may be used as a yttrium precursor. The structural formula of the "thd" is as follows.



thd

The pulsed aluminum precursor is chemically or physically adsorbed by the entire surface of the semiconductor substrate S. Since the aluminum precursor has reactivity with oxygen, when it is adsorbed by a material layer containing oxygen, it tends to change into an Al_2O_3 layer on the adsorption interface. In particular, the aluminum precursor chemically adsorbed by the exposed surface of the capacitor dielectric layer 110 containing oxygen as structural atoms reacts with the oxygen contained in the capacitor dielectric layer 110. As a result, an Al_2O_3 layer 200 is selectively formed on the exposed surface of the capacitor dielectric layer 110 at an atomic layer level. However, when the upper electrode 120 and the lower electrode 100 do not contain oxygen atoms, the aluminum precursor chemically or physically adsorbed by the exposed portions of the upper and lower electrodes 120 and 100 does not change into a metal oxide layer but remains as it is. Although not shown, when the upper or lower electrode 120 or 100 includes a conductive metal oxide layer such as an IrO_2 layer, an Al_2O_3 layer of an atomic layer level can be formed on the exposed portion of the conductive metal oxide layer included in the upper or lower electrode 120 or 100.

After forming the Al_2O_3 layer 200 only on the capacitor dielectric layer 110 at an atomic layer level by pulsing the aluminum precursor, the entire surface of the semiconductor substrate S is purged using inert gas. For example, the inert gas may be argon gas, and the purging time and flow rate of the inert gas may be 0.5-10 seconds and 50-300 sccm, respectively. When the entire surface of the

semiconductor substrate S is purged with inert gas, th aluminum precursor, which has physically adsorbed by the surfaces of the lower electrode 100 and the upper electrode 120, and the aluminum precursor, which has not reacted on the capacitor dielectric layer 110, are discharged from the reaction chamber. The aluminum precursor chemically adsorbed by the surfaces of the lower electrode 100 and the upper electrode 120 is not purged and mostly remains. However, in the embodiment of the present invention, the purging flow rate and time of inert gas can be appropriately adjusted to substantially remove the metal precursor adsorbed by the surfaces of the upper electrode 120 and the lower electrode 100.

The aluminum precursor pulsing step and the inert gas purging step constitute a one cycle of the atomic layer deposition process. The cycle is repeated until an Al_2O_3 layer 200' having a desired thickness is obtained. During the progress of succeeding cycles, an aluminum precursor reacts with oxygen atoms contained in the capacitor dielectric layer 110 in the manner of diffusion, so the Al_2O_3 layer 200 is continuously formed on the capacitor dielectric layer 110 at an atomic layer level. The aluminum precursor is just adsorbed by the surfaces of the upper electrode 120 and the lower electrode 100, and an Al_2O_3 layer is not formed thereon.

Meanwhile, an aluminum precursor usually contains hydrogen atoms. Accordingly, during a process of selectively forming an Al_2O_3 layer on the capacitor dielectric layer 110 using a method of manufacturing a semiconductor device according to the present invention, the dielectric characteristics of the capacitor dielectric layer 110 may be degraded. In particular, when the capacitor dielectric layer 110 is formed of a ferroelectric material such as a PZT layer or an SBT layer, the ferroelectric characteristics of the capacitor dielectric layer 110 may be degraded due to hydrogen contained in the aluminum precursor. For example, the remnant polarization value of the capacitor dielectric layer 110 may decrease. To recover the degradation of the capacitor dielectric layer 110 and enhance the dielectric characteristic such as the density of the Al_2O_3 layer, thermal treatment (see arrows) is performed in an oxygen atmosphere after the Al_2O_3 layer is formed on the capacitor dielectric layer 110 to a predetermined thickness.

The thermal treatment can be performed in a rapid thermal processing apparatus or a furnace type thermal processing apparatus. When the thermal treatment is performed in a rapid thermal processing apparatus, th temperature and time for the thermal treatment are 400-600°C and 10 seconds through 10 minutes.

Referring to FIG. 3, after the Al_2O_3 layer 200' is selectively formed only on the surface of the capacitor dielectric layer 110, as described above, an ncapsulating layer 210 which is another metal oxide layer directly spread on the entire surface of the semiconductor substrate S including the capacitor C is formed. Since the encapsulating layer 210 serves to prevent hydrogen from diffusing into the capacitor dielectric layer 110 during a succeeding InterLayer Dielectric (ILD) process, InterMetal Dielectric (IMD) process or passivation process, it is formed of a dense material layer. Since the semiconductor substrate S on which the encapsulating layer 210 is formed has the capacitor C on the surface thereof, it has a large surface topology. Accordingly, it is preferable to use an atomic layer deposition method for forming the encapsulating layer 210.

For example, when the encapsulating layer 210 is formed of an Al_2O_3 layer, it is defined that a step of pulsing aluminum source gas over the entire surface of the semiconductor substrate S, a step of purging with inert gas, a step of pulsing oxygen source gas, and a step of purging with inert gas constitute one cycle. The cycle is repeated until the encapsulating layer 210 is formed to a desired thickness.

One of the aluminum precursors mentioned above can be used as the aluminum source gas. H_2O gas, O_3 gas or N_2O gas may be used as the oxygen source gas. Argon gas may be used as the inert gas.

For example, when TMA gas, H_2O gas and argon gas are used as the aluminum source gas, the oxygen source gas and the inert gas, respectively, the pulsing time of the TMA gas is 0.1-2 seconds, the pulsing time of the H_2O gas is 0.1-2 seconds, the purging flow rate and time of the argon gas are 50-300 sccm and 1-10 seconds, and the temperature of the semiconductor substrate S is about 300°C.

In this first embodiment, an Al_2O_3 layer is selectively formed on the capacitor dielectric layer 110 using a method of manufacturing a semiconductor device according to the present invention. However, it will be apparent to those skilled in the art that an oxide layer containing Ta, Ti, Zr, Mg, Ce, Y, Nb, Hf, Sr or Ca may be formed on the capacitor dielectric layer 110. In this case, a metal precursor containing Ta, Ti, Zr, Mg, Ce, Y, Nb, Hf, Sr or Ca, which is widely known as having reactivity with oxygen, may be used in the aluminum precursor pulsing step of the first embodiment.

<Second Embodiment>

In a second embodiment, a method of manufacturing a semiconductor device according to the present invention is applied to a process of forming a contact in a semiconductor device.

Referring to FIG. 4, in the second embodiment of the present invention, a semiconductor substrate S including a predetermined conductive region 220 which does not contain oxygen, an interlayer insulation layer 230 which is spread on the conductive region 220 and contains oxygen, and an opening 240, which exposes the conductive region 220, is prepared. The conductive region 220 may be the upper or lower electrode of a capacitor, a gate electrode, a bit line, a word line, or the lower conductive line of a multi-layered interconnection layer. The interlayer insulation layer 230 may be a silicon oxide layer or a silicon oxynitride layer.

Subsequently, an Al_2O_3 layer is formed as a selective metal oxide layer 250 only on the exposed surface of the interlayer insulation layer 230 using an atomic layer deposition method in the same manner as used in the first embodiment. It is obvious that like the first embodiment, an oxide layer containing Ta, Ti, Zr, Mg, Ce, Y, Nb, Hf, Sr or Ca may be formed on the exposed surface of the interlayer insulation layer 230.

In the second embodiment like the first embodiment, thermal treatment can be performed in an oxygen atmosphere after the selective metal oxide layer 250 is formed to enhance the dielectric characteristic of the selective metal oxide layer 250.

As in the second embodiment described above, when the metal oxide layer 250 is selectively formed only on the exposed surface of the interlayer insulation layer 230, the metal oxide layer 250 can prevent substance, which can degrade a semiconductor device, from diffusing below the metal oxide layer 250 during a succeeding process of forming a predetermined material layer on the interlayer insulation layer 230.

Hereinafter, technical effects accomplished when a method of manufacturing a semiconductor device according to the present invention is applied to a process of encapsulating a capacitor of a semiconductor memory device will be described in detail by explaining test examples.

<Test Example 1>

A stack type capacitor pattern, in which a Pt layer (a lower electrode), a PZT layer (a capacitor dielectric layer) and an Ir/IrO_2 layer (an upper electrode) are sequentially stacked, was formed on a semiconductor substrate. Thereafter, the

semiconductor substrate was loaded in an atomic layer deposition apparatus, and a stabilizing step was performed such that the pressure of a chamber was maintained at 0.1-1 torr, and the temperature of the semiconductor substrate was maintained at about 300°C. Next, the cycle of an atomic layer deposition process according to the first embodiment of the present invention was repeated 100 times, and a test sample was obtained. Here, TMA gas was used as an aluminum precursor, and the pulsing time in each cycle was about 0.1 second. Argon gas was used as purge gas, and the purging time in each cycle was about 1 second. After obtaining the sample through the above series of steps, an X-ray photoelectron spectroscopy (XPS) analysis was performed on the sample to check whether an Al_2O_3 layer was formed on the capacitor dielectric layer. The result of the analysis is shown in FIG. 5. In FIG. 5, the horizontal axis denotes binding energy, and the vertical axis denotes arbitrary intensity. Referring to FIG. 5, an aluminum 2p peak (see III) indicating the binding energy between aluminum and oxygen is observed. Accordingly, it can be confirmed that an Al_2O_3 layer is selectively formed on the capacitor dielectric layer of the sample. In particular, since oxygen source gas was not pulsed, it can be inferred that oxygen contained in the Al_2O_3 layer is supplied from the capacitor dielectric layer.

<Test Example 2>

A capacitor pattern was formed on a semiconductor substrate under the same conditions as the first embodiment, and a sample 1 and a sample 2 were separately manufactured. Thereafter, the following processes were sequentially performed on the samples 1 and 2, and the remnant polarization values of their capacitor dielectric layers were measured whenever each process was completed. The results of the measurement are shown in FIG. 6. In FIG. 6, the horizontal axis denotes the processes performed on the samples 1 and 2, and the vertical axis denotes the remnant polarization values.

-Sample 1

In step A_1, an Al_2O_3 layer was selectively formed on a capacitor dielectric layer according to the first embodiment of the present invention. The process conditions of step A_1 are almost the same as those in the test example 1. Thereafter, in step A_2, a semiconductor substrate was loaded in a rapid thermal processing apparatus and thermal-treated for 10 seconds at a temperature of 700°C in an oxygen atmosphere. Next, in step A_3, an encapsulating layer wrapping the

capacitor pattern was formed of an Al_2O_3 layer according to the first embodiment. Here, TMA gas, H_2O gas and argon gas were used as aluminum source gas, oxygen source gas and purge gas, respectively. The pulsing time of the TMA gas was 0.5 seconds. The pulsing time of the H_2O gas was 0.3 seconds. The purging time and purging flow rate of the argon gas were 6 seconds and 150 sccm. The temperature of a wafer was 300°C.

-Sample 2

In step B_1, a semiconductor substrate including a capacitor pattern was loaded in a rapid thermal processing apparatus and thermal-treated. The process conditions of step B_1 were the same as those of step A_2. Thereafter, in step B_2, an encapsulating layer wrapping the capacitor pattern was formed of an Al_2O_3 layer. Here the process conditions of step B_2 were the same as those of step A_3.

Referring to FIG. 6, in the case of the sample 1, the remnant polarization value of the capacitor dielectric layer decreases a little due to the influence of the TMA gas and the H_2O gas, which contain hydrogen. However, the remnant polarization value increases over the initial value after the step A_2 of performing a rapid thermal process in an oxygen atmosphere. Although the remnant polarization value decreases a little after the step A_3 of encapsulating a capacitor, the decreased remnant polarization value is almost the same as the initial value. In the case of the sample 1, the remnant polarization value rarely decreased even though the TMA gas and the H_2O gas containing hydrogen were used in step A_3.

In the case of the sample 2, the remnant polarization value of the capacitor dielectric layer increases over the initial value after the step B_1 of performing a rapid thermal process in an oxygen atmosphere. However, the remnant polarization value greatly decreases after the step B_2 of encapsulating a capacitor, compared to the sample 1.

The sample 1 is different from the sample 2 in that it has a selective metal oxide layer which has been thermal-treated in an oxygen atmosphere. The fact that the remnant polarization value in the sample 1 did not decrease unlike the sample 2 even if the sample 1 had undergone the step A_3, in which hydrogen-base gas was supplied, suggests that the thermal treated selective metal oxide layer effectively blocked hydrogen not to diffuse into the capacitor dielectric layer. Accordingly, it is obvious that the thermal treated selective metal oxide layer blocks diffusion of

hydrogen into the capacitor dielectric layer in succeeding ILD process, IMD process and passivation process.

Although the invention has been described with reference to a particular embodiment, it will be apparent to one of ordinary skill in the art that modifications of the described embodiment may be made without departing from the spirit and scope of the invention. For example, the spirit of the present invention can be applied when selectively forming a metal oxide layer only on the exposed surface of a gate oxide layer in a gate electrode pattern having a gate oxide layer therebelow.

[Effect of the Invention]

According to the present invention, a metal oxide layer can be selectively formed only on an insulation layer containing oxygen. In particular, when a method of manufacturing a semiconductor device according to the present invention is applied to a process of encapsulating a capacitor of a semiconductor memory device using an atomic layer deposition method, the degradation of a capacitor dielectric layer can be prevented even if source gas containing hydrogen is used. In addition, degradation of a capacitor dielectric layer due to hydrogen during an ILD process, an IMD process or a passivation process, which is performed after the capacitor encapsulating process, can be effectively prevented.